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Random Waveform Using Digital Multiplexer

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Abstract: **Waveform generator is an important component in digital electronics and its applications. Need of different waveforms from a single clock is the basic idea of waveform generator.In this paper we are presenting a Random waveform circuit based on a digital multiplexer. It is a programmable waveform generator that changes the output sequence depending upon the input 16 bit code from a microcomputer. The output is a binary sequence in reflection to the input. We can generate 2^{16} binary sequences. The circuit is built around 16 to 1 multiplexer whose selection varies periodically depending upon the input master clock, generating random and sequential output.**

Keywords: **binary, sequential, clock, Multiplexer, latches, serial, parallel, simulation, microcomputer.**

1. INTRODUCTION

A waveform generator is a piece of electronic test equipment used to generate electrical waveforms either analog or digital. These waveforms can be repetitive, periodic, single shot or sequential, excited by an internal trigger. A random square wave generator is capable of generating a varied sequence of binary patterns with variable parameters such as frequency and duty cycle. The frequency depends upon the master clock. A square wave itself is a non-sinusoidal periodic waveform in which amplitude alternates between the fixed maximum and minimum values. Square waves are often encountered in electronics and signal processing. It stochastic counterpart is a two state trajectory. Square waves (periodic or non-periodic) use a timing reference or "clock signals". They seem to be composed of single frequency but their frequency response shows that they comprise of a large number of harmonics.Square wave generators are usually by the combination of analog and digital components. It involves using digital signal processing, waveform synthesis, DAC or ADC. In this paper we are presenting a digital based random/sequential square wave generator.

2. CIRCUIT

The circuit is built around a 16 to 1 digital multiplexer. The 4-bit sequential counter and two 8-bit clocked latches are also employed .A master clock is generated from a signal generator. The simulation and circuit design is done in NI MultiSim 12.0.

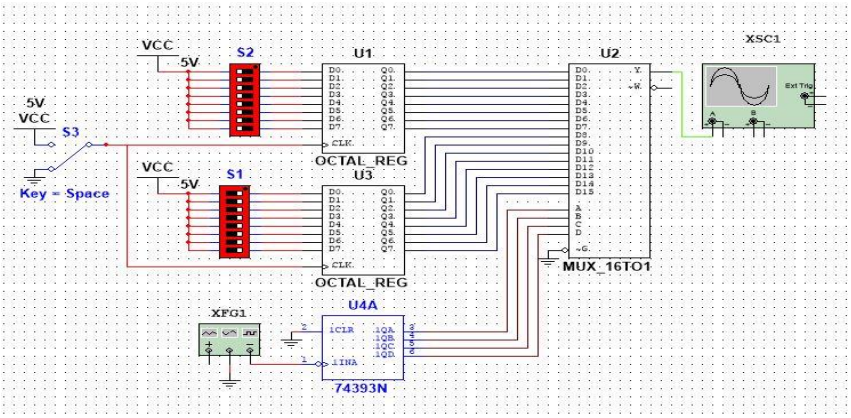

Fig.1: Main circuit diagram

Octal_Reg is the 8-bit latch, 74393N is 4-bit counter. The circuit works on 5-V DC. The 16-bit input is distributed to the two 8-bit latches via the 2 8-bit DIP switches for sake of simplicity. Otherwise the 16-bit input is to come from a PC or microcomputer depending upon the circuit design an alternate design is also given below with changes in the latch. 74ALS373N is added with no clock or enable feature.

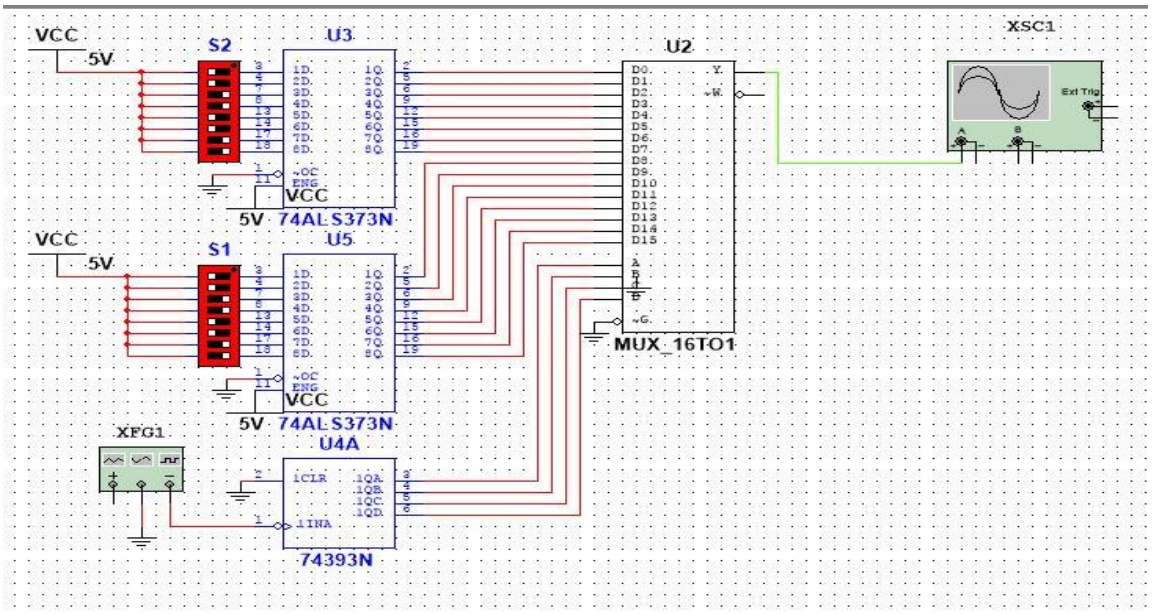

Fig.2: Alternate circuit diagram

3. WORKING

The circuit is a random square wave generator using a 16 to 1 multiplexer. The binary sequence at the output Y of the multiplexer can be programmed. The two DIP switches are shown in place of the control bits from a pc. When an input is received at the latches a control signal is given as low to high at the clk input of the latches (or registers), with this the input 16-bit data is put on the multiplexer input and no new data is entertained until clk goes H to L again.

XFG1 is a signal generator used as a master clock. It is referenced at 50 KHz and 5 V vpp. This acts as the input clock of the 4-bit counter whose outputs 1QA-1QD are connected to the select lines A-D of the 16 to 1 multiplexer. As soon as the clock starts, counter runs from 0000 to 1111 selecting all the 16 inputs of the multiplexer sequentially to output. This continues until a sequence is fed to the multiplexer via the latches.

Depending upon the input 16-bit code the output sequence is chosen. We can have 2^{16} sequences at the output out of which 6 are sequential, that are 1010101010101010, 1100110011001100, 1111000011110000 ,1111111100000000, 11111111111111111 ,0000000000000000, these sequences are nothing but the frequency divided square waves of the master clock. Therefore along with random sequence generation we can get ½ , ¼ , 1/8 , 1/16 of the master clock.

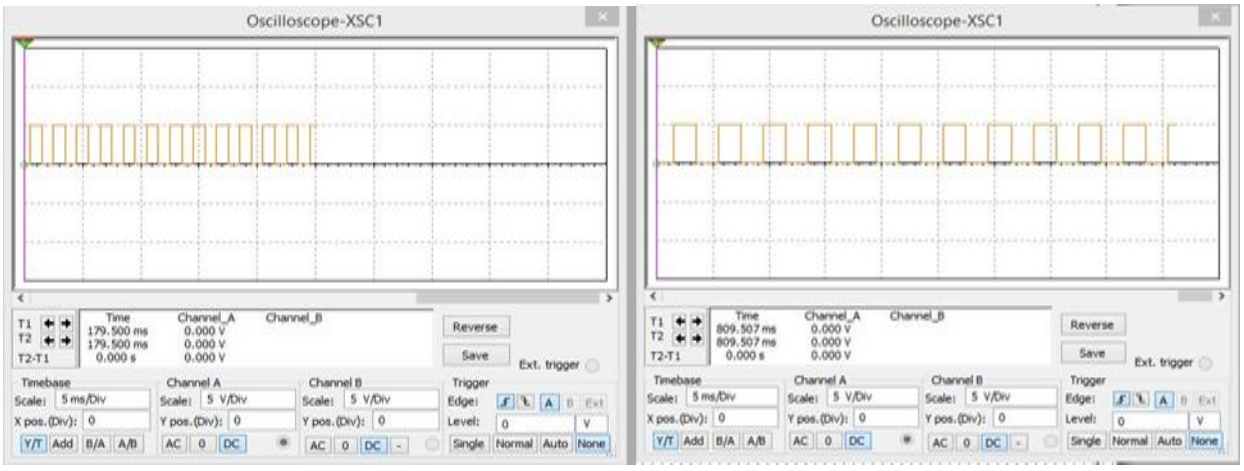

Fig.3: Output waveform for 1010101010101010 and 1100110011001100

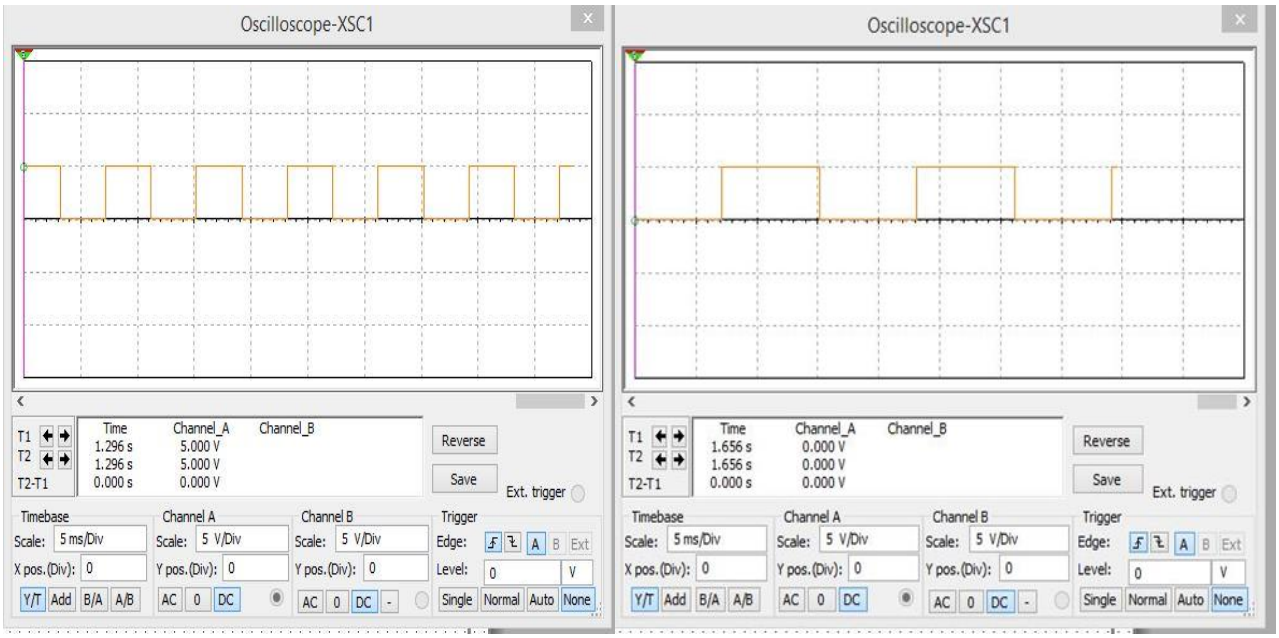

Fig.4: Output waveform for 1111000011110000 and 1111111100000000

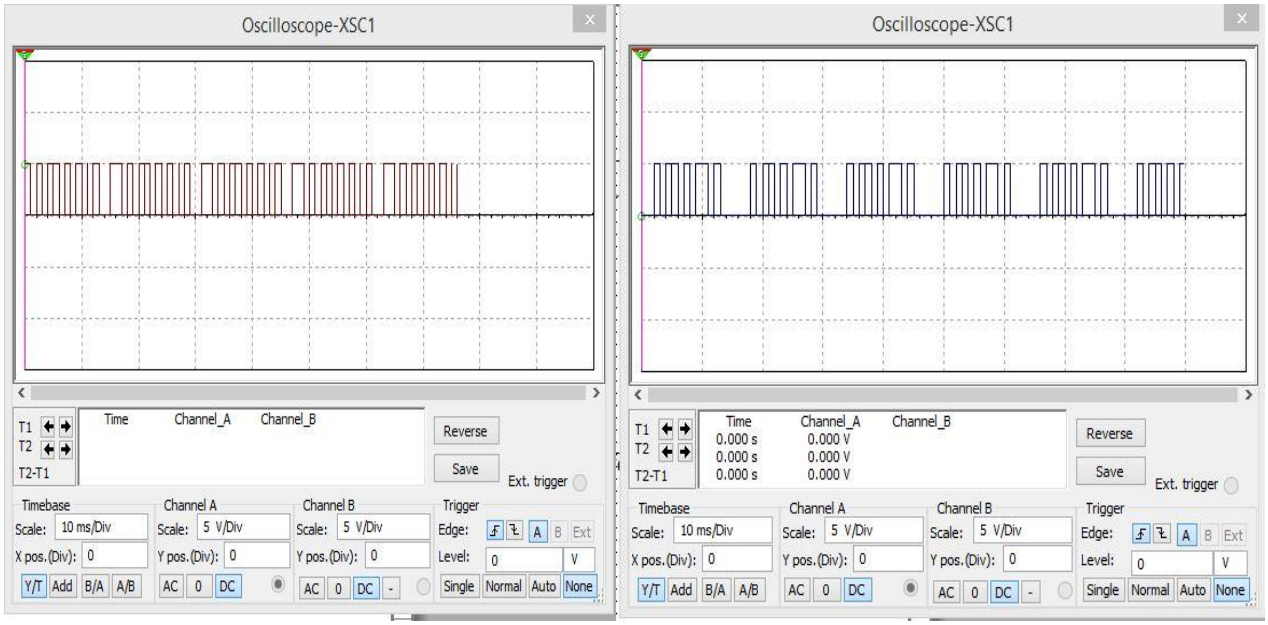

Fig.5: Random sequence 0010100101011011 and 1110100101001011

4. CONCLUSION

In this work a design of random/sequential waveform generator was under research. One promising application of such devices is in signal generators. The main goal was to development sufficiently compact, low cost waveform generator using digital components. Circuit designs and different topologies were explored to choose the best suitable variant to comply with the required purpose. It appeared that a 16 to 1 mux was the best choice of design as it provides enough flexibility and speed to the device. They were simulated with taking into account the influence of losses in real components. Master clocks can be chosen at appropriate values so as to allow synchronous operation with other devices.

It appeared that the device can also be used a data transfer device as parallel to serial transfer module. Parallel data from one system can be transferred to another system or stored serially. The speed depends upon the clock speed.

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